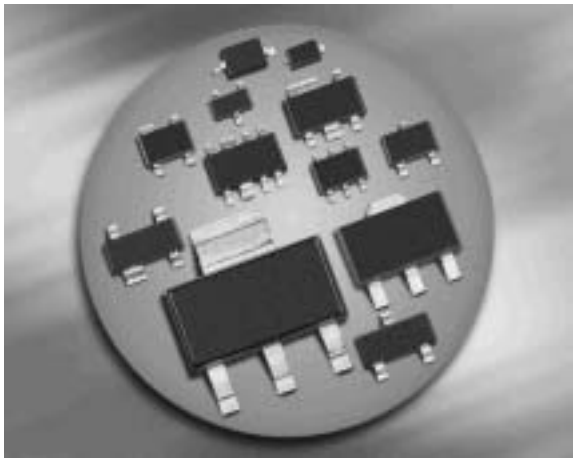
Silicon PIN Diode



- Optimized for low current antenna switches in hand held applications
- Very low forward resistance (typ. 1.5 Ω @ I_F = 1 mA)
- Low capacitance at zero volt reverse bias at frequencies above 1 GHz (typ. 0.28 pF)
- Very low signal distortion
- Pb-free (RoHS compliant) package[1)]
- Qualified according AEC Q101

BAR88-02LRH **BAR88-07LRH** **BAR88-099LRH** **BAR88-098LRH**
BAR88-02V

Type	Package	Configuration	L_S(nH)	Marking
BAR88-02LRH	TSLP-2-7	single, leadless	0.4	U8
BAR88-02V	SC79	single	0.6	U
BAR88-07LRH	TSLP-4-7	parallel pair, leadless	0.4	T8
BAR88-098LRH	TSLP-4-7	anti-parallel, leadless	0.4	98
BAR88-099LRH	TSLP-4-7	anti parallel, leadless	0.4	S8

[1]Pb-containing package may be available upon special request

Maximum Ratings at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Value	Unit
Diode reverse voltage	V_R	80	V
Forward current	I_F	100	mA
Total power dissipation	P_{tot}		mW
BAR88-02LRH, -07LRH $T_S \leq$ 133°C		250	
BAR88-02V, $T_S \leq$ 123°C		250	
BAR88-098LRH, -099LRH $T_S \leq$ 133°C		250	
Junction temperature	T_j	150	°C
Operating temperature range	T_{op}	-55 ... 125	
Storage temperature	T_{stg}	-55 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point[1)]	R_{thJS}		K/W
BAR88-02LRH, -07LRH		≤ 65	
BAR88-02V		≤ 105	
BAR88-098LRH, -099LRH		≤ 65	

Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Breakdown voltage $I_{(BR)}$ = 5 µA	$V_{(BR)}$	80	-	-	V
Reverse current V_R = 60 V	I_R	-	-	50	nA
Forward voltage	V_F				V
I_F = 1 mA		-	0.75	0.9	
I_F = 100 mA		-	0.95	1.2	

[1]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

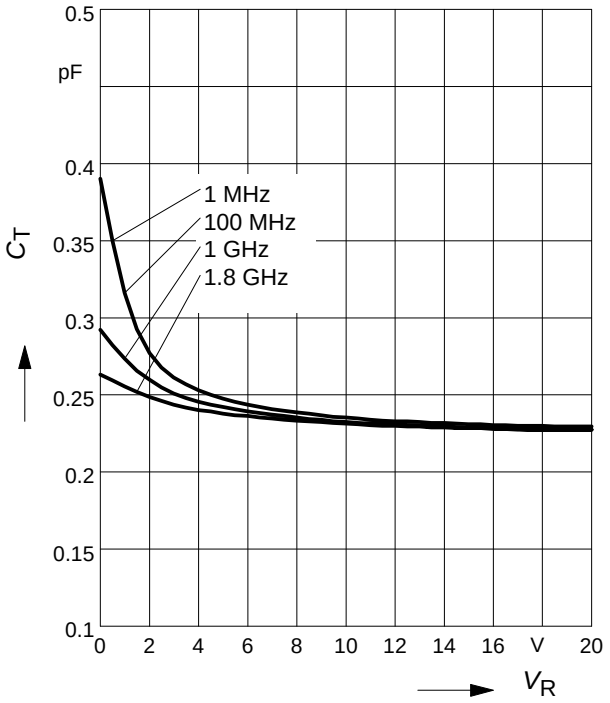
Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics					
Diode capacitance	C_T				pF
V_R = 1 V, f = 1 MHz		-	0.3	0.4	
V_R = 0 V, f = 100 MHz		-	0.4	-	
V_R = 0 V, f = 1 GHz		-	0.28	-	
V_R = 0 V, f = 1.8 GHz		-	0.25	-	
Reverse parallel resistance	R_P				kΩ
V_R = 0 V, f = 100 MHz		-	65	-	
V_R = 0 V, f = 1 GHz		-	2.5	-	
V_R = 0 V, f = 1.8 GHz		-	1.5	-	
Forward resistance	r_f				Ω
I_F = 1 mA, f = 100 MHz		-	1.5	2.5	
I_F = 5 mA, f = 100 MHz		-	0.8	-	
I_F = 10 mA, f = 100 MHz		-	0.6	-	
Charge carrier life time	τ_{rr}	-	500	-	ns
I_F = 10 mA, I_R = 6 mA, measured at I_R = 3 mA, R_L = 100 Ω					
I-region width	W_I	-	13	-	µm
Insertion loss[1)]	I_L				dB
I_F = 1 mA, f = 1.8 GHz		-	0.11	-	
I_F = 5 mA, f = 1.8 GHz		-	0.07	-	
I_F = 10 mA, f = 1.8 GHz		-	0.06	-	
Isolation[1)]	I_{SO}				
V_R = 0 V, f = 0.9 GHz		-	15	-	
V_R = 0 V, f = 1.8 GHz		-	11	-	
V_R = 0 V, f = 2.45 GHz		-	9	-	

[1]BAR88-02LRH in series configuration, Z = 50Ω

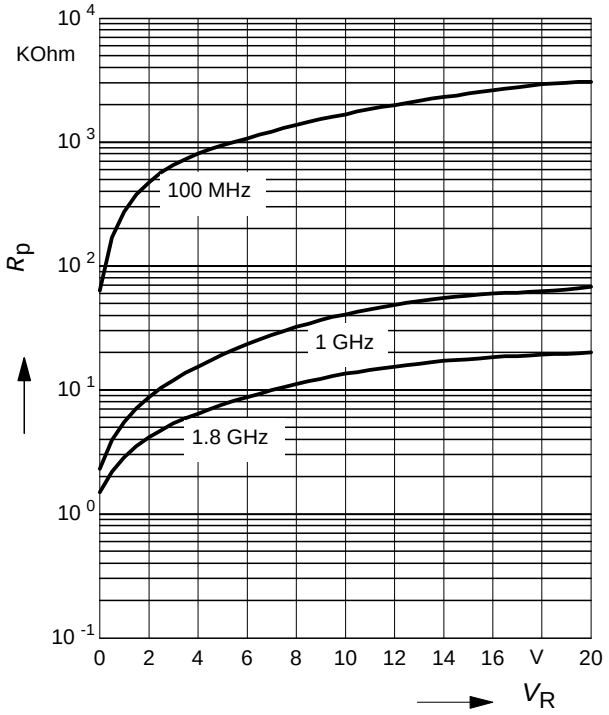
Diode capacitance $C_T = f\ (V_R)$

f = Parameter



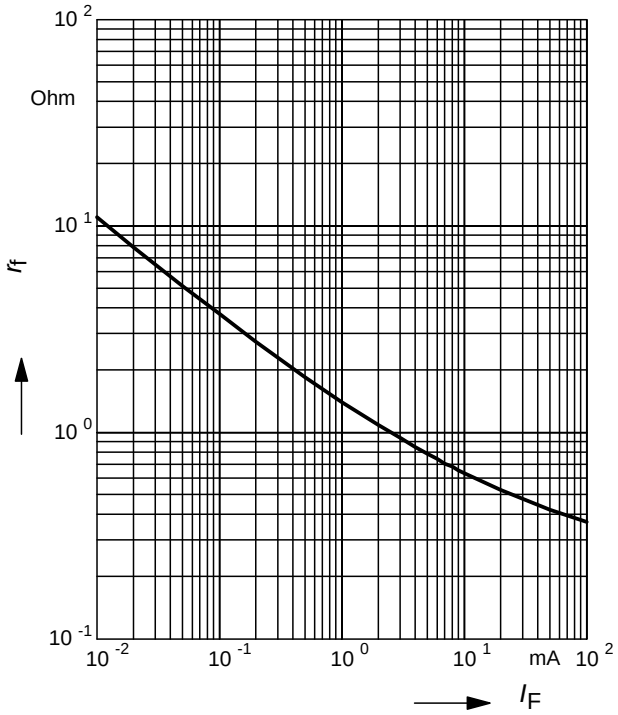
Reverse parallel resistance $R_P = f(V_R)$

f = Parameter



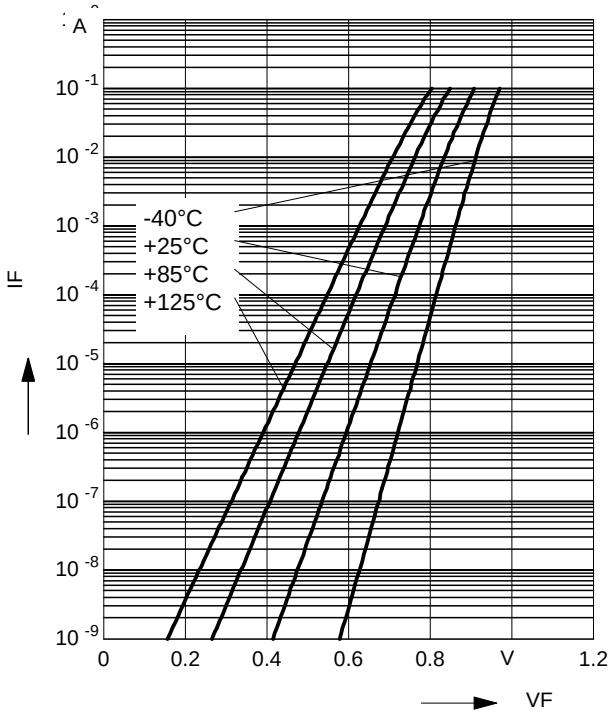
Forward resistance $r_f = f\ (I_F)$

f = 100MHz

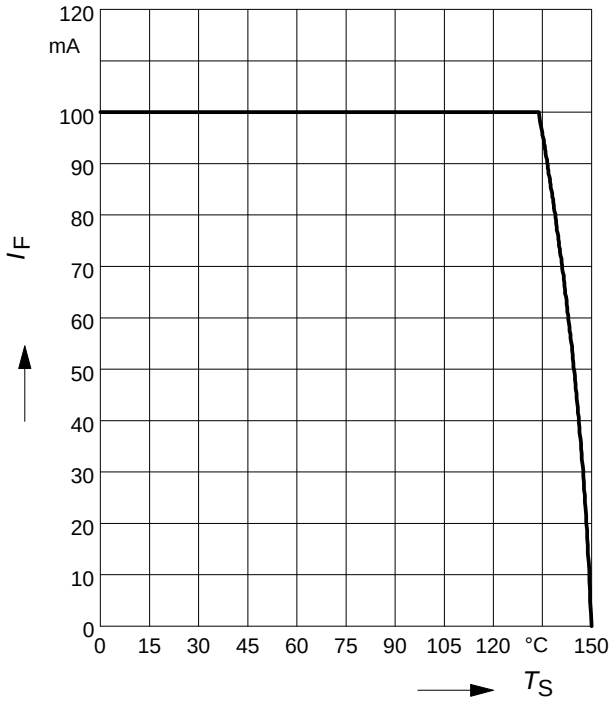


Forward current $I_F = f\ (V_F)$

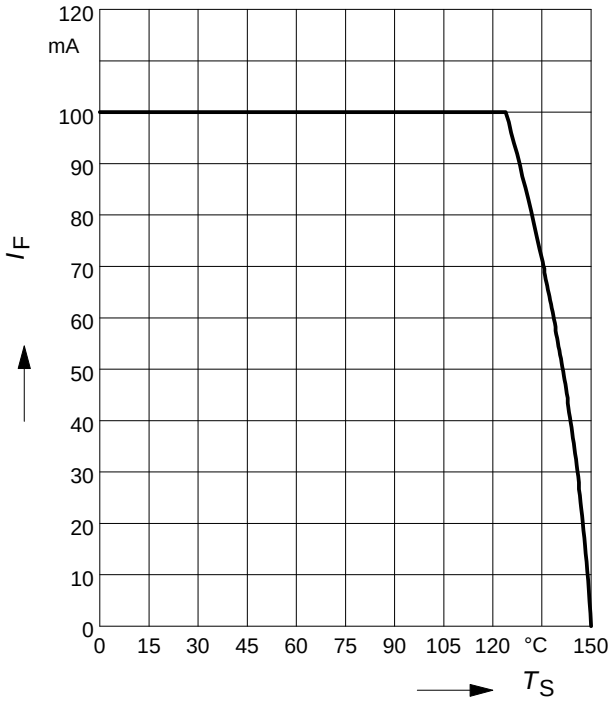
T_A = Parameter



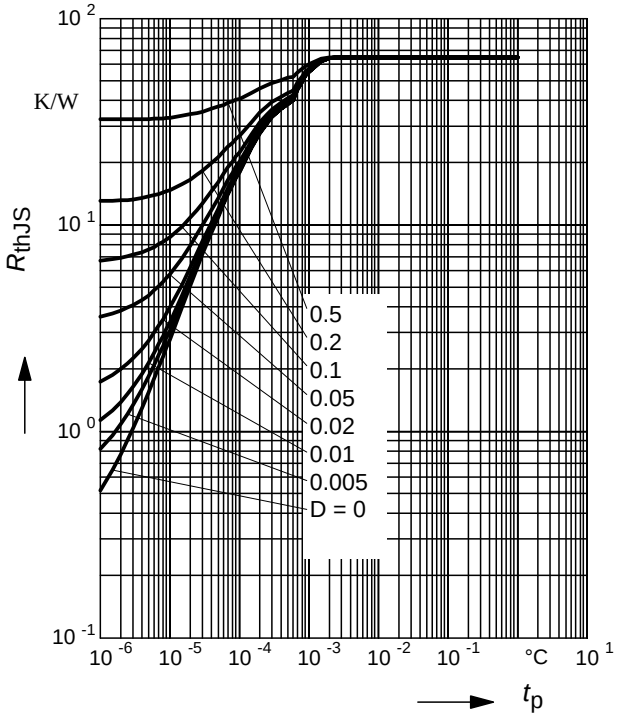
Forward current $I_F = f(T_S)$
BAR88-02LRH, -07LRH,
-098LRH, -099LRH



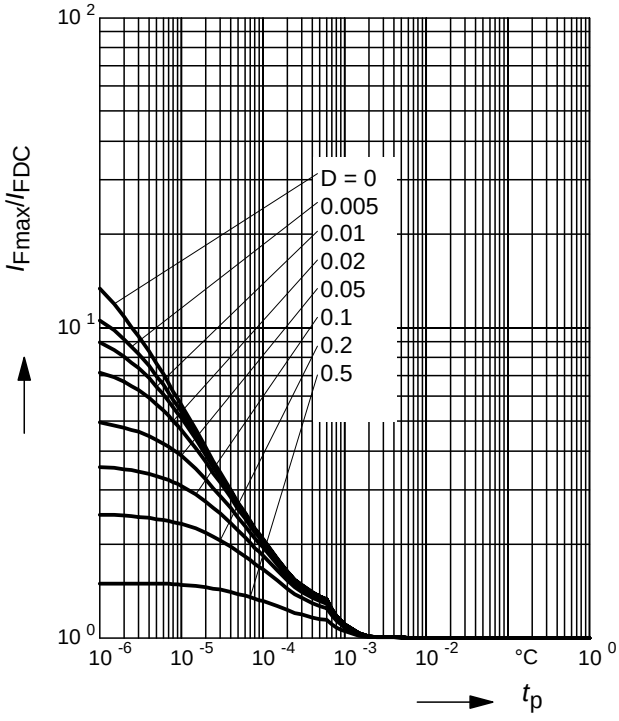
Forward current $I_F = f(T_S)$
BAR88-02V



Permissible Puls Load $R_{thJS} = f(t_p)$
BAR88-02LRH, -07LRH
-098LRH, -099LRH

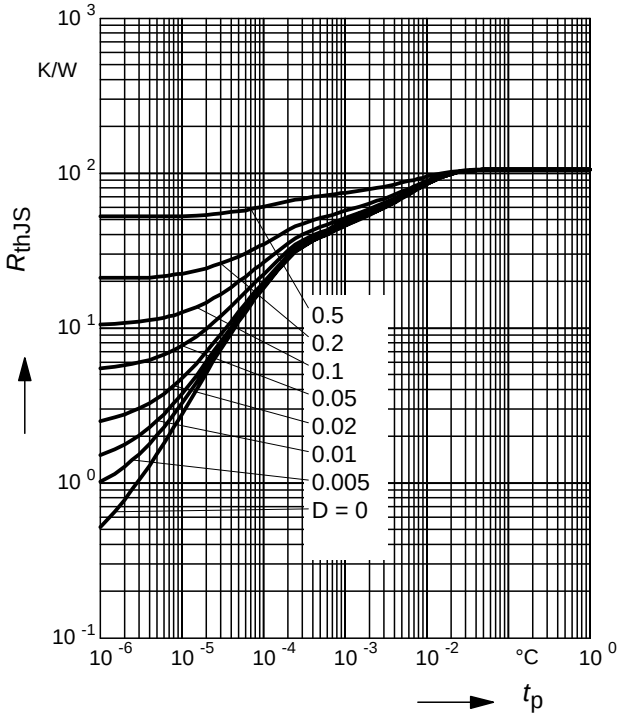


Permissible Pulse Load
$I_{Fmax}/I_{FDC} = f(t_p)$, BAR88-02LRH
-07LRH, -098LRH, -099LRH



Permissible Puls Load $R_{thJS} = f(t_p)$

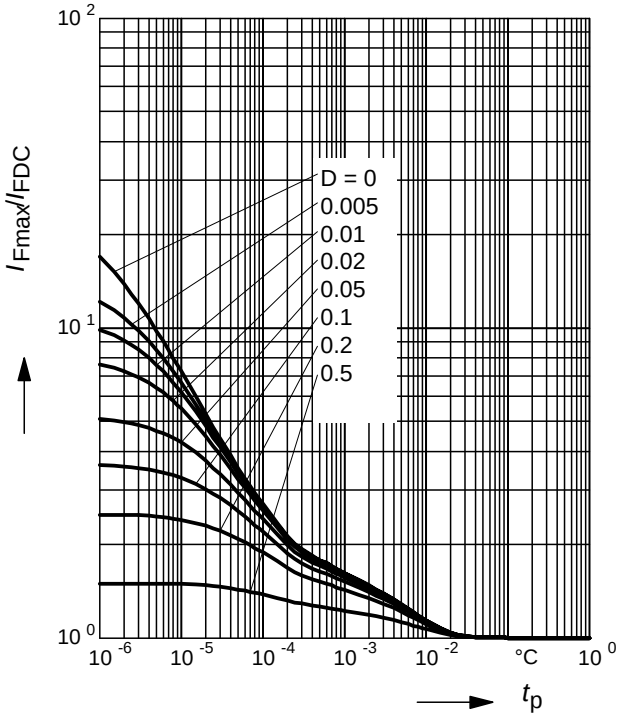
BAR88-02V



Permissible Pulse Load

$I_{Fmax}/I_{FDC} = f(t_p)$

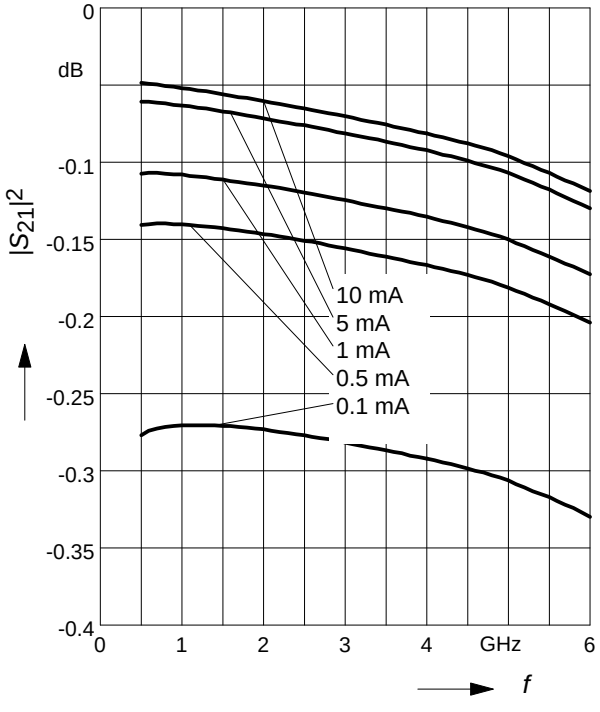
BAR88-02V



Insertion loss $I_L = -|S_{21}|^2 = f(f)$

I_F = Parameter

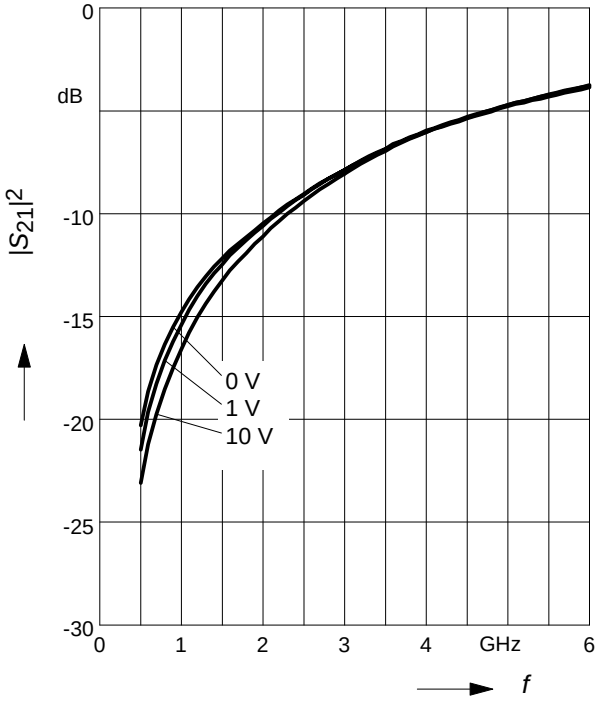
BAR88-02LRH in series configuration, Z = 50Ω



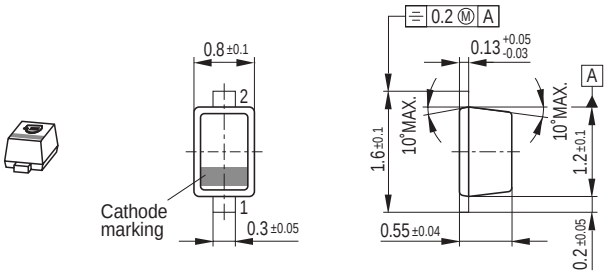
Isolation $I_{SO} = -|S_{21}|^2 = f(f)$

V_R = Paramter

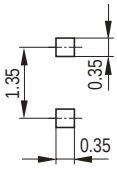
BAR88-02LRH in series configuration, Z = 50Ω



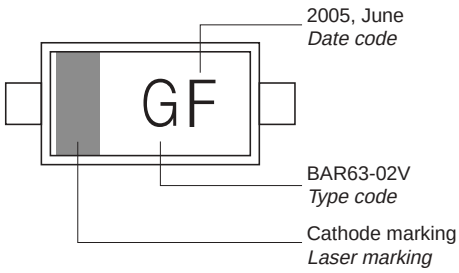
Package Outline



Foot Print

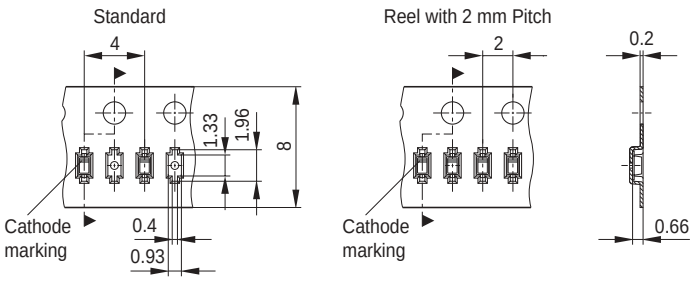


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø180 mm = 8.000 Pieces/Reel (2 mm Pitch)
Reel ø330 mm = 10.000 Pieces/Reel

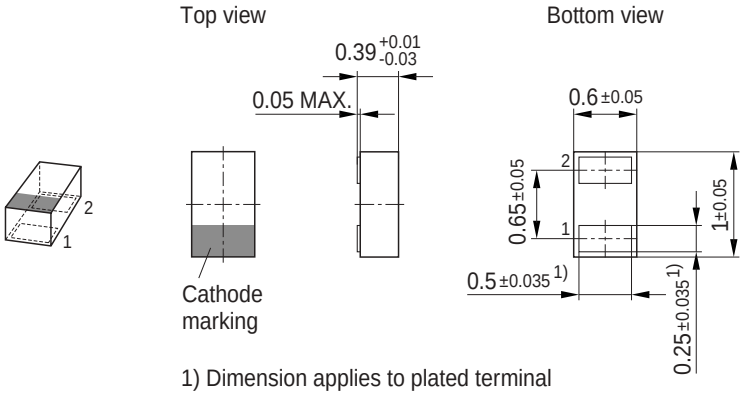


Date Code marking for discrete packages with one digit (SCD80, SC79, SC75[1)]) CES-Code

Month	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
01	a	p	A	P	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5	n	3	N	5

1) New Marking Layout for SC75, implemented at October 2005.

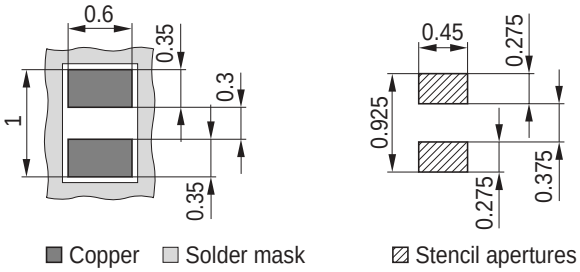
Package Outline



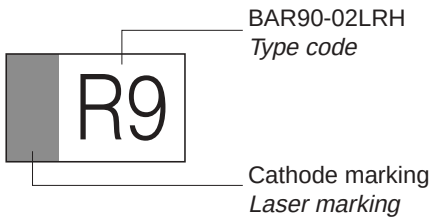
1) Dimension applies to plated terminal

Foot Print

For board assembly information please refer to Infineon website "Packages"

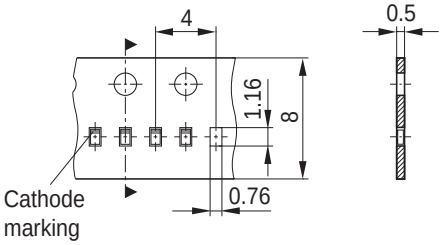


Marking Layout (Example)

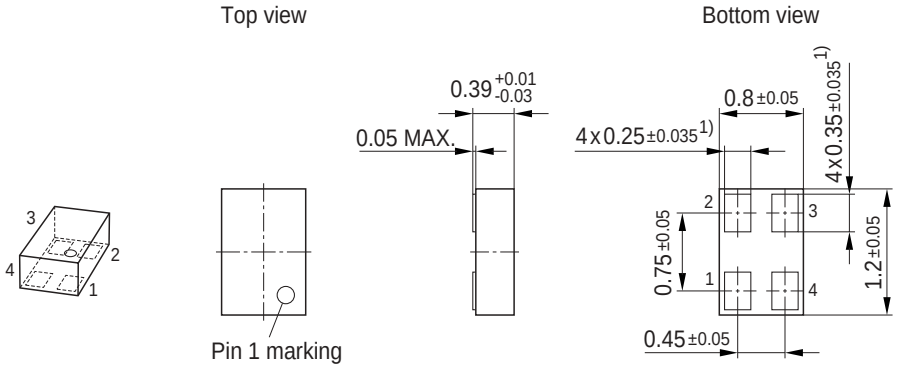


Standard Packing

Reel ø180 mm = 15.000 Pieces/Reel
Reel ø330 mm = 50.000 Pieces/Reel (optional)



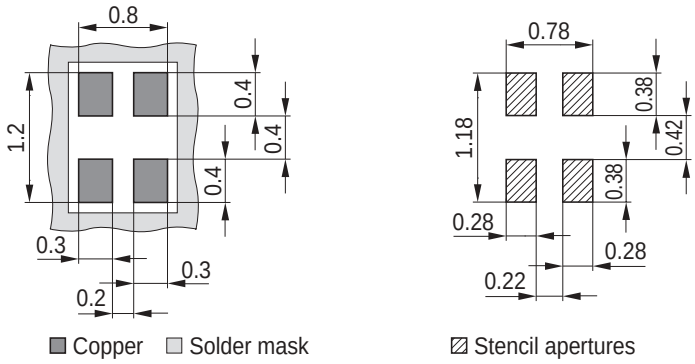
Package Outline



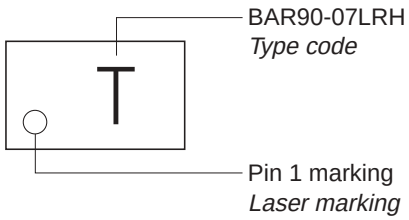
1) Dimension applies to plated terminal

Foot Print

For board assembly information please refer to Infineon website "Packages"

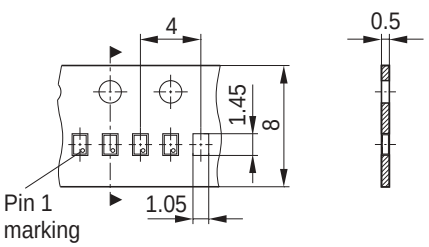


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 15.000 Pieces/Reel



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